VXI Overview

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VXI Overview

A Proven High Performance Instrument Architecture
VXIbus (VMEbus Extensions for Instrumentation) (IEEE-STD-1155)

Developed in 1987 to provide a standard modular open industry architecture for instrumentation.

Intended to provide:

- **High-density platform through shared resources**
- **Precise timing coordination between instruments**
- **Longer system support through multi-vendor solutions**
- **Capability to address high-performance requirements**

VXIbus Basics

A VXIbus system or subsystem consists of a mainframe, VXIbus devices, a slot 0 card, resource manager, and host controller.

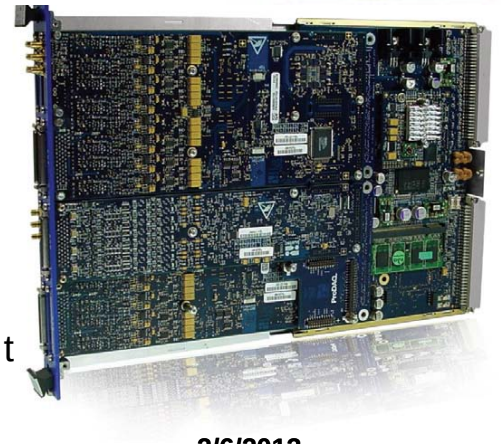
- **VXIbus Devices:**
  Typically message-based or register-based devices

- **VXIbus Mainframe:**
  Houses the VXIbus devices (4,5,6 and 13 slot mainframes)
  Contains the power and cooling mechanism
  Contains the communication backplane

- **Slot 0 Interface:**
  Backplane management and (Shared) System Clock sources
  Arbitration
  Remote control through various comm interfaces

- **Resource Manager:**
  Configures the modules for proper operation at power-up and reset

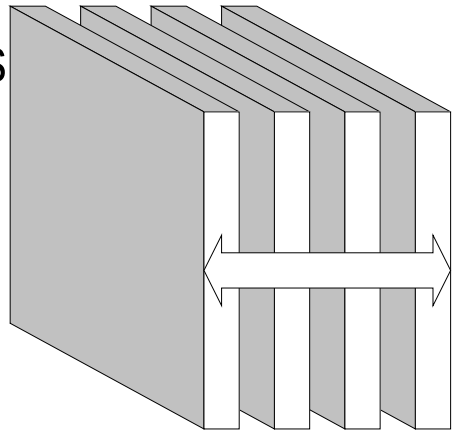
- **Host Controller:**
  Controls the operations of the ATE system and environment



Specification Overview *Electrical*

The VXIbus specifies has two primary backplane connectors (P1 and P2). The P1 connector, (mandatory in VME or VXIbus), carries the data transfer bus. The P2 connector, expands the data transfer bus to a full 32-bit size, and adds:

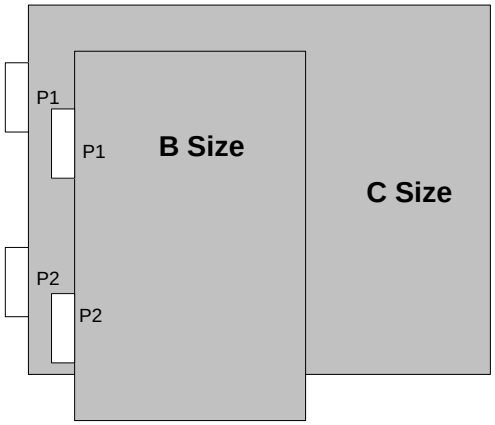
- Four additional power supply voltages
- The local bus
- Analog sumbus
- TTL and ECL trigger buses
- 10 MHz differential ECL clock signal



Specification Overview *Mechanical*

P1 16-bit data VMEbus
24-bit addressing
+ 5, + /-12 Volts

P2 32-bit data VMEbus
10 MHz clock bus
Analog sum bus
12-pin local bus
TTL/ECL trigger buses
-5.2, -2, + /-24 Volts



- **C-size cards allow for the addition of EMC/EMI shielding**
- **Industry's most common and widely supported modular footprint is the C-size card**
- **One unique logical address (LA) per VXIbus device, allowing for 256 LAs in a single VXIbus system**
- **Other platforms (i.e. M-modules, PMC, PXI, VME) can be accommodated through the use of adapters**

	Size	Spacing
C Size	23.3 x 34 cm (9.2 x 13.4 in.)	3 cm (1.2 in.)
B Size (VME)	23.3 x 16 cm (9.2 x 6.3 in.)	2 cm (0.8 in.)

Specification Overview *Power & Cooling*

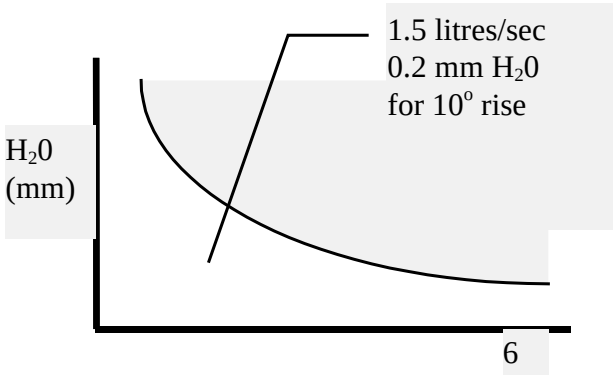
P1

Volts P1	Qty Pins P1	Power P1
GND	8	
+ 5V	3	15W
+ 12V	1	12W
-12V	1	12W

P2

Volts P2	Qty Pins P2	Power P2	Power P1& P2
GND	18		
+ 5V	4	20W	35W
+ 12V			12W
-12V			12W
+ 24V	1	24W	24W
-24V	1	24W	24W
-5.2V	5	26W	26W
-2V	2	4W	4W

- The VXIbus mainframe is specified for power delivered. Each power supply has a peak DC current delivery and peak-to-peak dynamic current delivery.
- By calculating the total power and current of modules within the system, the total system power can be determined.
- The VXIbus mainframe specifies worst-case pressure drops vs. airflow rate through a single slot.
- Each instrument must specify airflow and back pressure required (normally for a 10°C rise in temperature). System cooling can be determined by plotting on a mainframe graph.
- Optimize mainframe for cooling/power. Remember that more cooling extends component life.

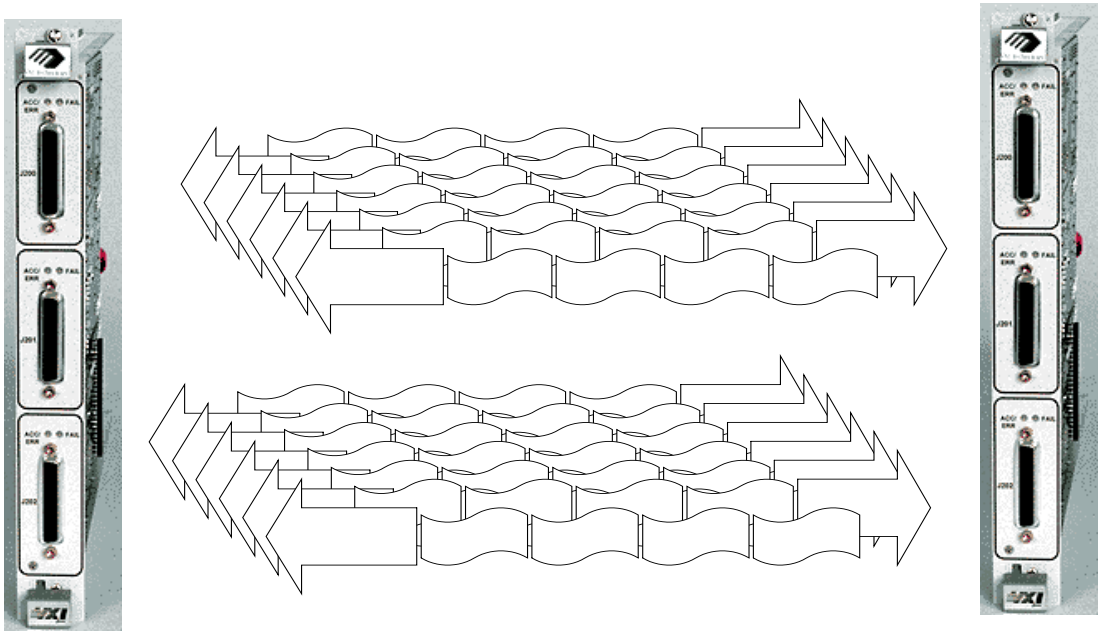


Specification Overview *Power & Cooling*

- **Power - VXI added power supplies above VME specifications**
  - **+5 V DC - Main power source for most VXI Instruments**
  - **+/- 12 V DC - Used for powering analog devices, communications interfaces**
  - **+/- 24 V DC - Used for powering analog signal sources (20V into hi Z) plus +/- 15 V regulators**
  - **-5.2 V DC - For ECL devices**
  - **-2 V DC - Used for the termination of ECL loads**
  - **+5 V DC STDBY - Standby for memory / power lost**

Specification Overview *EMI/EMC*

The VXIbus specifies radiated and conducted EMC limits for both generation and susceptibility. This ensures that modules containing sensitive electronic circuits perform to expectations without interference from any other module operating in the system.

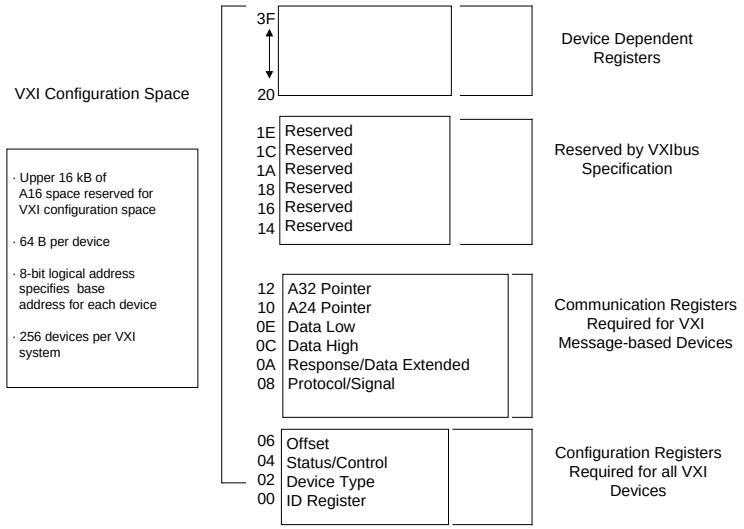


Communicating with the VXIbus Instruments

Hardware Communications:

- External computer to VXIbus chassis interface:
  GPIB/VXI, MXI2/VXI, USB 2.0/VXI, Firewire/VXI, LAN/VXI, PCIe/VXI, etc.
  PC-platform and OS independent

- Embedded computer:
  Resides in the slot 0, generally PC- or PPC based



Two main ways to communicate with a VXIbus device:

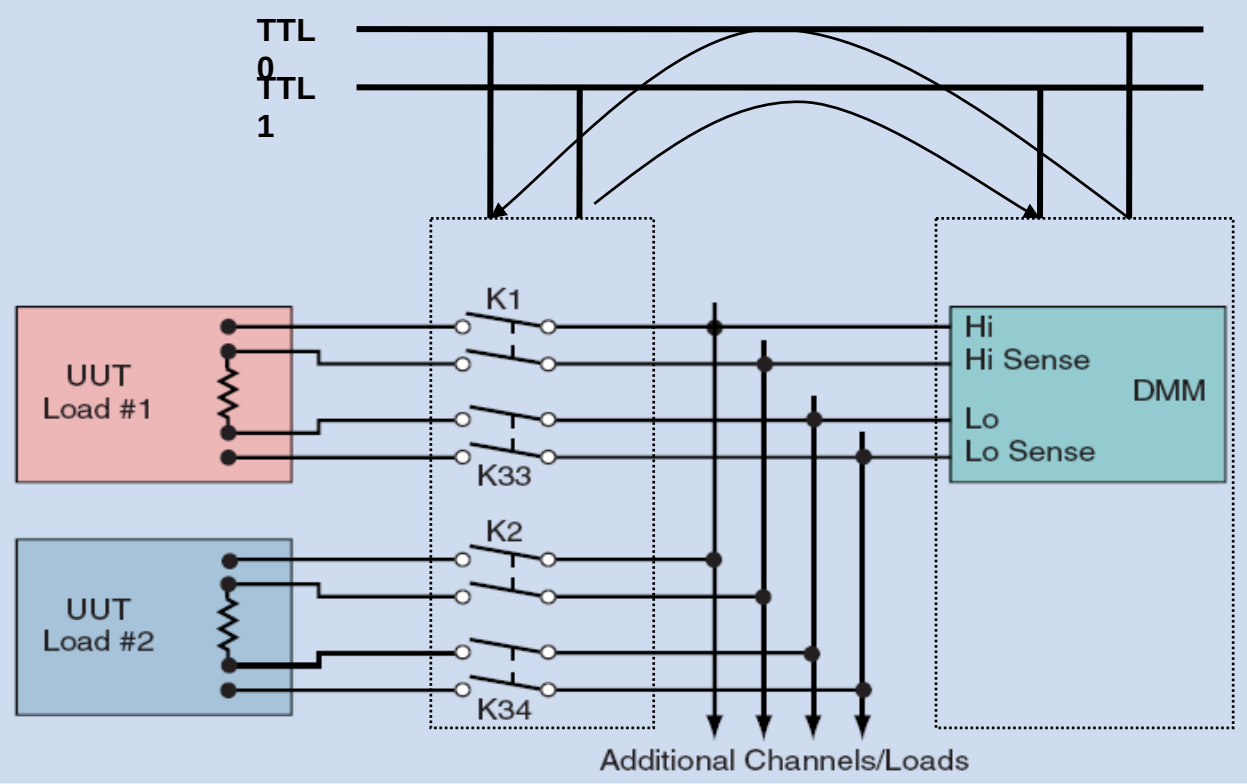
- **Message-based devices**
  The message-based device has a Word Serial Protocol to allow ASCII-level communications. SCPI builds upon this. Relatively low throughput

- **Register-based devices**
  The register-based device communicates only through register reads and writes. Configuration is controlled by VXIbus-defined configuration registers but programmed through device dependent registers. Up to 320MB/sec throughput

VXI plug&play drivers use the VISA protocol to provide an API that is communications bus agnostic.

Using the Trigger Bus *Application*

- TTL0 – DMM measure complete, close next relay channel
- TTL1 – Relay has settled, initiate DMM measurement

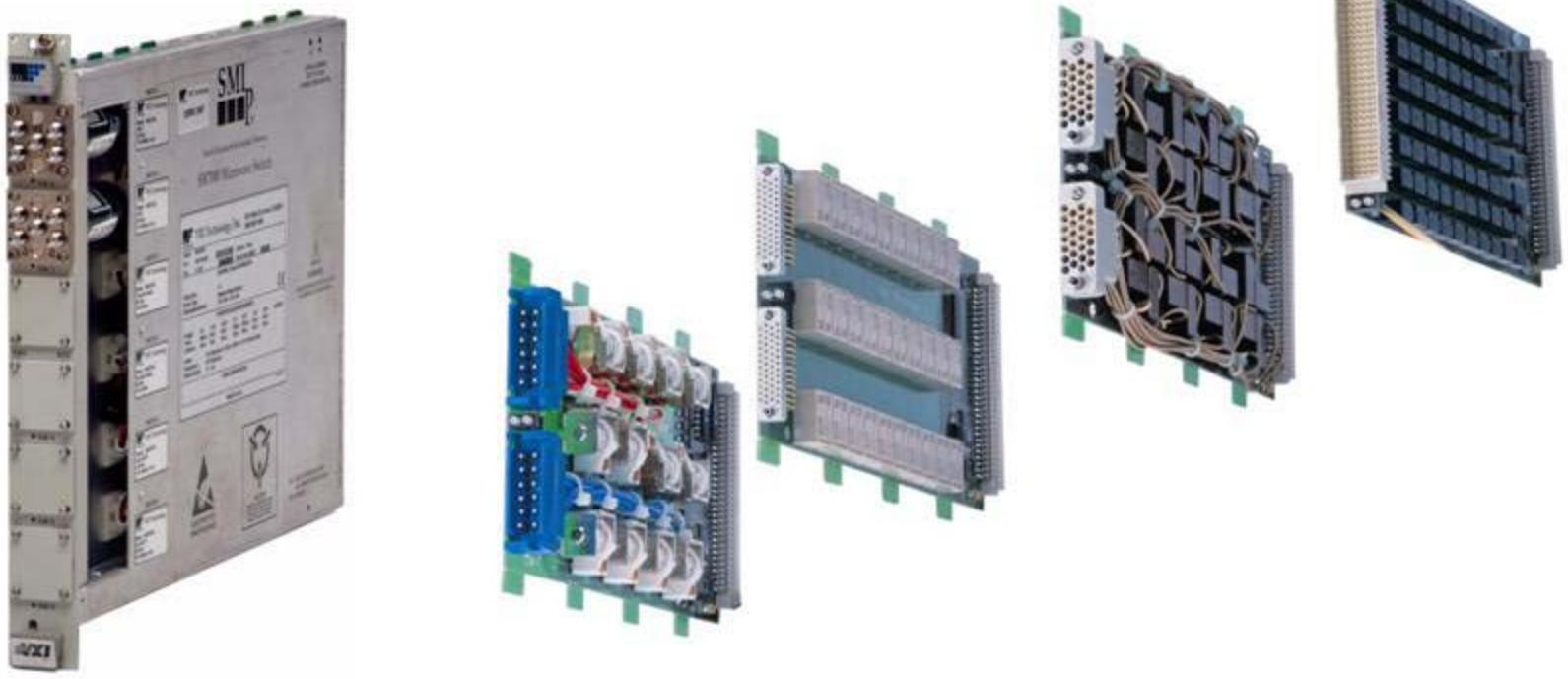


- Highly deterministic asynchronous handshaking **significantly** reduces test time by removing any dependency on host controller to manage the switch/measure sequencing

Connectors

Mechanical

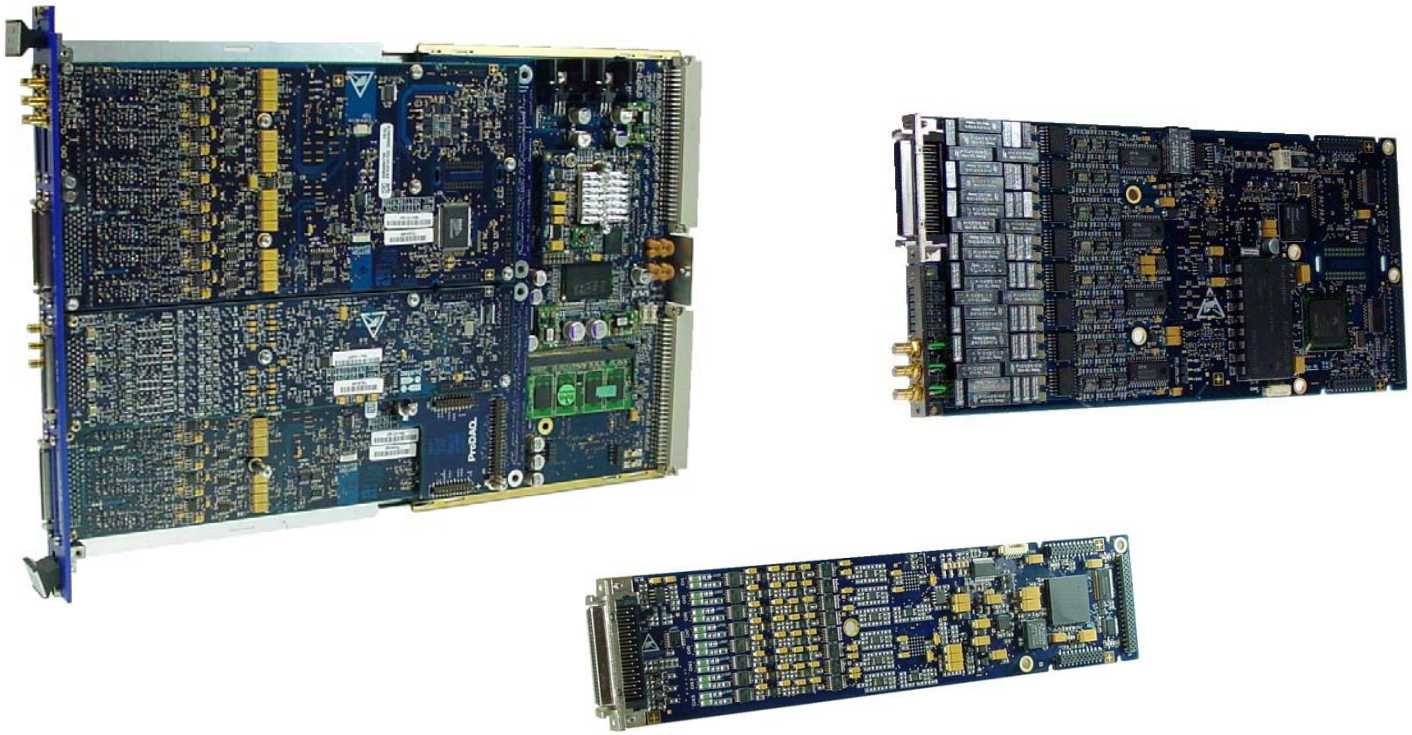
- **1.2” Center spacing permits use of larger components, and more robust, ergonomically friendly connectors**
  - 6 x 6 RF matrix (18 GHz) in two slots
  - (20) SPST 30 A relays in one slot
  - (144) 2-wire crosspoint, 2 A switched relays in ½ slot



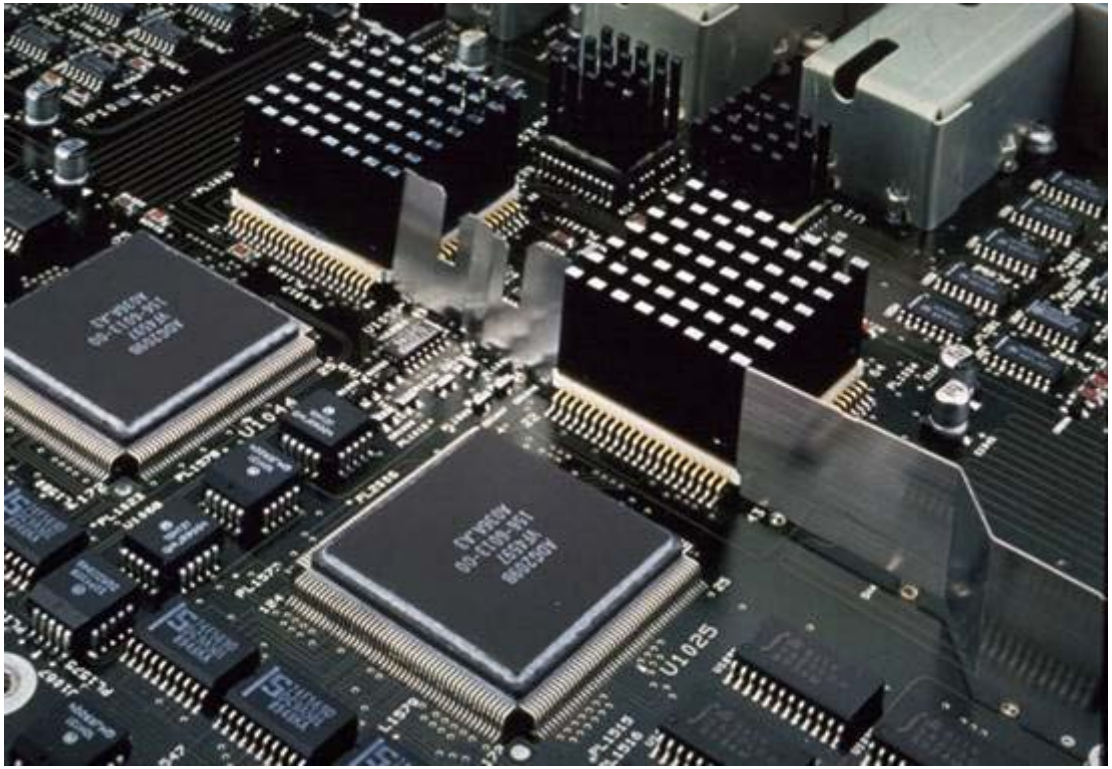
Density

Mechanical

- **1.2” Center spacing permits higher density and multiple functions per slot**
  - Up to 8 different functions per slot
  - Up to 384 digital I/O channels per slot
  - Up to 128 high presicion 24-bit Sigma-Delta ADC channel per slot (52 kS/s/ch)



Larger Components = Robust Designs



Flexible Remote Control

The VXIbus can attribute its longevity in part to its ability to adapt to newer communication bus architectures for remote control without affecting backward compatibility.

PCI-VXI

USB 2.0-VXI

PCIe-VXI

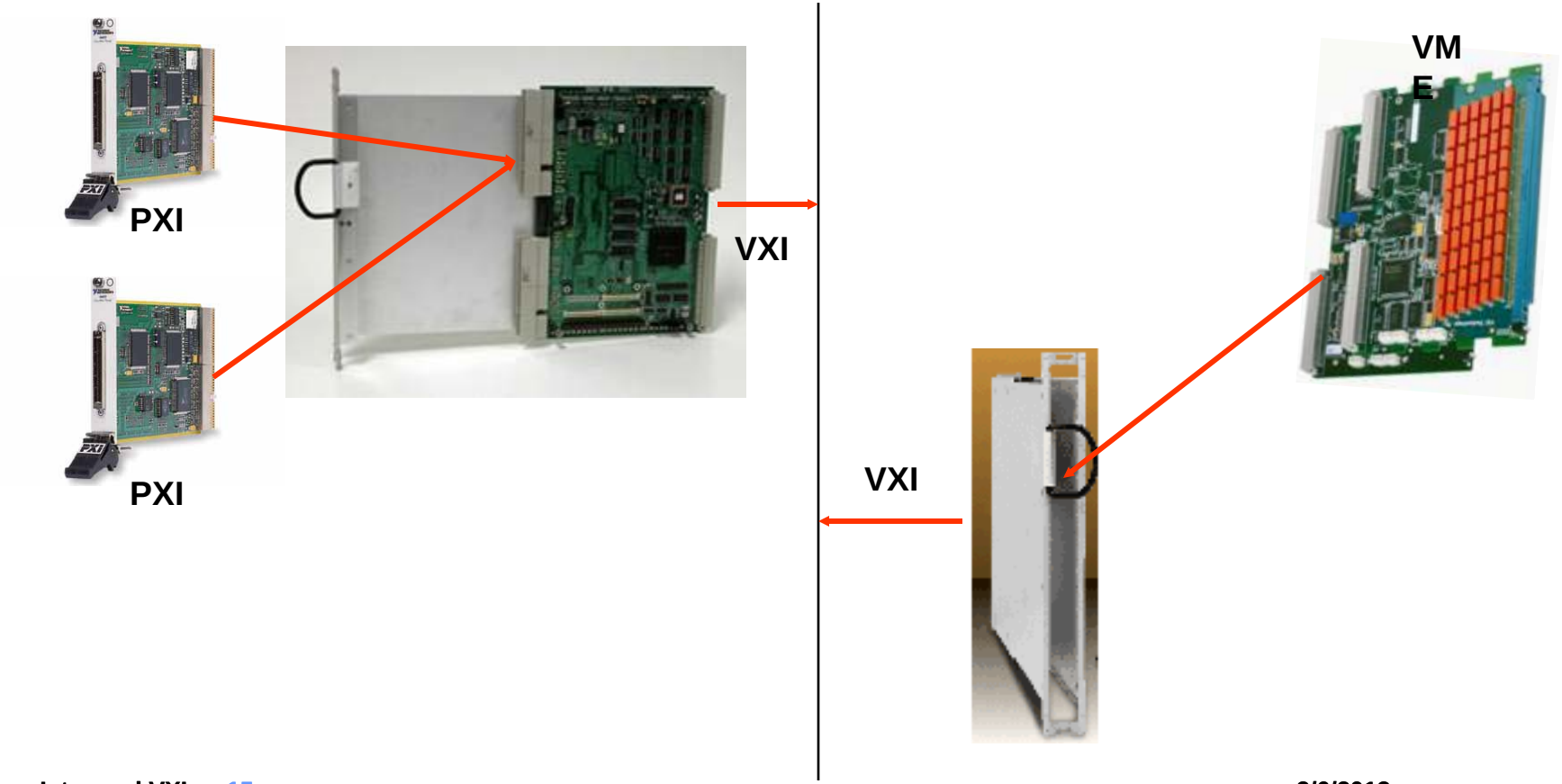
GPIB-VXI

IEEE1394-VXI

LXI-VXI

A Platform that Unites

- VXI adapts many platforms via carriers in a single mainframe
  - Can eliminate need for multiple mainframes within a system



Module within a module platform

The VXIbus specification permits multiple 'sub-modules'.

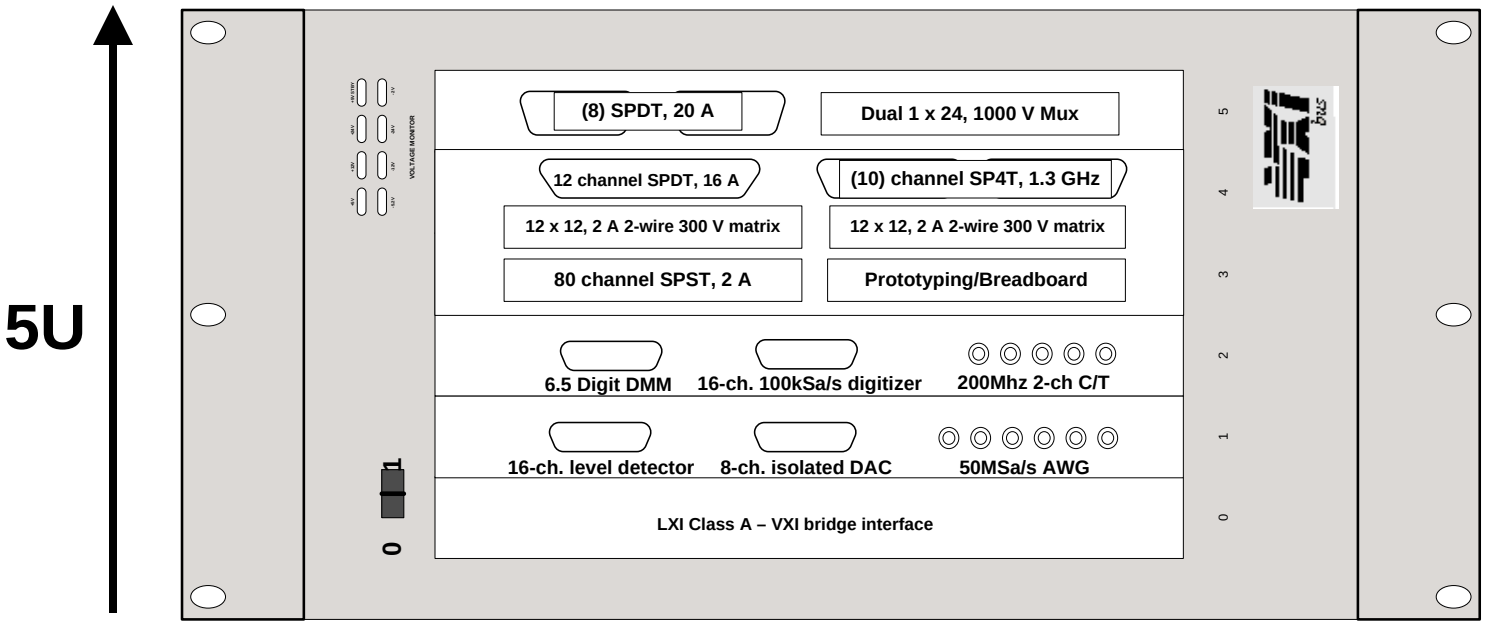
- Each can be treated as an independent instrument with discrete logical address.

Enables very high-density, flexible system

- 6.5 Digit DMM
- 200 MHz Dual Channel Counter/Timer
- 50 MSa/s AWG

- 6 unique functions in two slots

VXIbus Capability in Small Footprint



SYSTEM DEFINITION, 6-slot VXI Mainframe (5U)

Host Communication Interface, LXI-VXI bridge
16 channel 100 V threshold detector/interrupter
8 channels, independent, isolated DAC, 32 V dc/0 – 20 mA
50 MSa/s Arbitrary Waveform/Function Generator
6.5 Digit DMM
16 channel 16-bit independent 100 kSa/s ADC (40 V)
Dual Channel 200 MHz Counter/Timer

(80) SPST, 300 V/2 A relays
Prototyping breadboard
12 x 24, 300 V/2 A matrix (two modules)
(10) SP4T 50 Ohm Coaxial Trees, 1.3 GHz
(12) SPDT, 16 A, 300 W dc relays
(8) SPDT, 20 A, 600 W dc relays
(2) 1 x 24 1000 V multiplexers

VXI Bus Consortium 2012

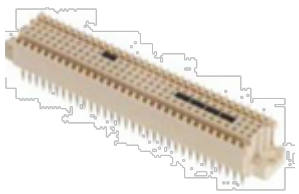
- **VXIbus Consortium owns, develops and promotes the VXI standard**
- **Vendors continue to introduce new VXI products**
  - Many are also investing in designing out obsolescence of legacy products
- **Four pillars of VXI messaging**
  - **Well Conceived –** Created by leading test and measurement companies, the VXI bus is a well defined and open industry standard.
  - **Established** – With a 25 year history of success, VXI has established itself as the most prevalent modular instrumentation bus.
  - **Time Tested** – VXI is the de-facto standard for applications that have long life cycle requirements. The VXI test platform will outlive the device it was originally designed to test.
  - **Thriving** – As significant investment in the new development on the platform continues, VXI is thriving. Its flexibility allows VXI to play a key role in hybrid systems that also PXI, LXI, and GPIB components.
- **VXI Technical Working Group completed the VXI 4.0 specs in 2010**
  - **Tracks VME specification for enhancements**
    - VITA 1.5-2003, 2eSST
    - VITA 41, VSX (VME Switched Serial)

VXIBus – Looking Forward

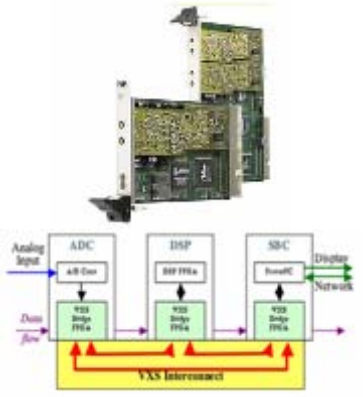
- **Initiative**
  - VXI Consortium has introduced the 4.0 specification
- **VXI 4.0**
  - Represents quantum leap in capability over 3.0
  - Maintains backward compatibility to preserve investment of large installed base
- **Opportunity**
  - Continue to be the modular platform of choice for large scale test and data acquisition applications
  - Integrate other modular platforms through adapters
  - Center spacing, power, board real estate for more robust designs that exist in current rev of spec

Goals of VXI 4.0

- **Compatible with Legacy VXI**
- **VITA 1.5-2003; 5-Row Connector**
  - More Power Lines
    - Support for 3.3 V Logic
  - More Return Lines
    - Greater noise immunity for advanced designs
  - Incorporates 2eSST for 320MB/s parallel and synchronous transfers
  - Additional Clock/Sync Lines
- **VITA-41 (VXS)**
  - Incorporates P0 connector for switched serial comms
  - Potential for >20 GB/s throughput (GenII)
  - Design Flexibility
    - Transparent adaptations of cPCI, PXI & PXI Express modules with simple carriers and VME for DSP/CPU, etc.

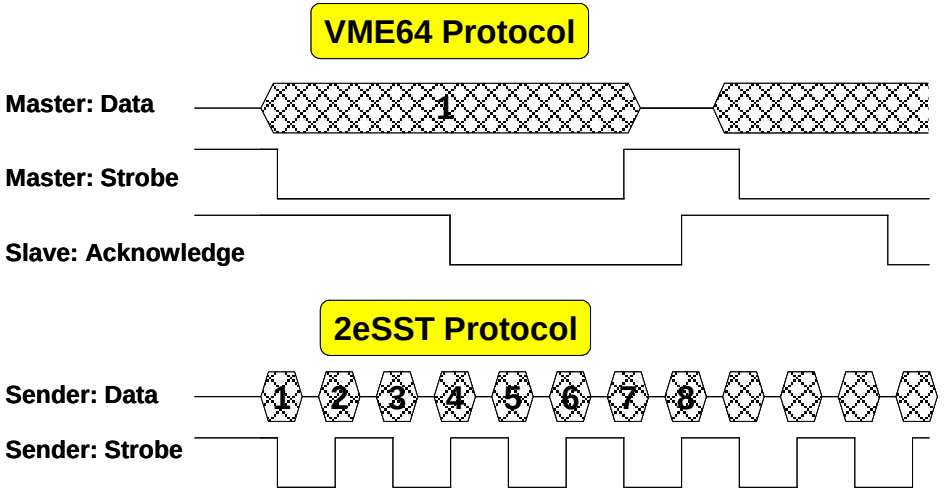


PCI EXPRESS



VITA 1.5-2003; 2eSST

2eSST Protocol:

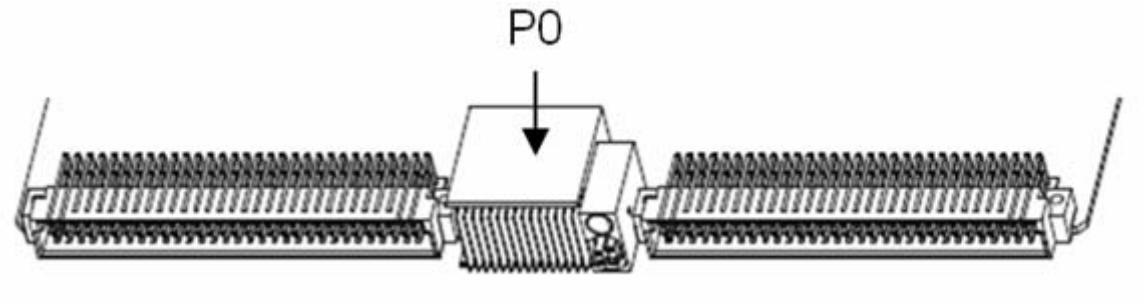


- **Two-edge Source Synchronous Transfers:**
  - No acknowledge from slave, slave must be able to accept/provide data at given rate
  - Data is transferred on both edges of strobe signal
- **Defined data rates of 160, 267 and 320 MB/s**
- **Allows for broadcast data transfers**

VITA 41; VXS (VME Switched Serial)

- **VITA-41: Adds P0 connector for differential, serial buses for multi-lane, high speed links**
  - Connector does not interfere with existing P1 and P2 connectors
  - Dual x4 links are defined by VITA-41.4
  - Future Expansion: Up to x32 can be defined later

New VITA-41 Differential
Serial Bus Connector



The Benefits of the Specification Update

- **Protects Your Investments:**
  - **A newly relevant specification adds capability to VXI applications while maintaining backward compatibility with previous revisions**
- **Provides a Future Path:**
  - **One of most powerful modular instrument platforms**
- **Produces Solutions:**
  - **Extends the VXI track record as the primary test solution when:**
    - The price of failure is very high
    - The products that are being tested have a long life cycle and need a test platform is not prone to obsolescence
    - Reduced size, open standard, interoperable, fast, and cost-effective solution required
    - C-size VXI is the perfect card geometry

What Application Spaces Benefit from VXI 4.0?

Digital Test:

Provides more power and throughput for today's high speed serial and parallel bus architectures

Data Acquisition:

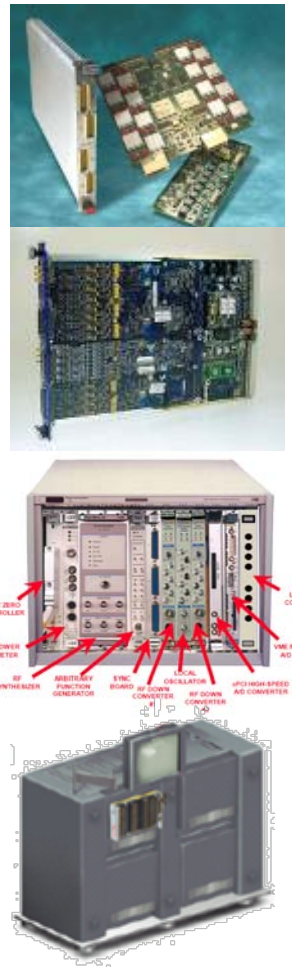
Provides more cumulative throughput across the communications bus

Synthetic Instruments:

Provides point to point communications for IF/RF acquisition and generation

SIGINT, EW and Radar:

Need more power and high speed paths between measurement and processing blocks



VXI 4.0 Summary

- VXI-1 Rev. 4.0 enhancements make VXI one of the world's most powerful instrumentation busses for many years to come
- Maintains backwards compatibility with existing VXI modules
- Is an IEEE standard
- No obsolescence problems like in PC related busses
- A high-end packaging solution for military/aerospace test, high-speed digital, RF, synthetic, and data acquisition applications